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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/893,566 | 06/29/2001 | Joon-Ha Park | 8733.454.00 | 5094 |

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MCKENNA LONG & ALDRIDGE LLP
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| EXAMINER | |
|---|---|
| NGUYEN, JENNIFER T | |
| ART UNIT | PAPER NUMBER |
| 2674 | |

DATE MAILED: 08/12/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/893,566 | PARK ET AL. | |
| | Examiner | Art Unit | |
| | Jennifer T Nguyen | 2674 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 June 2001*.

2a)☑ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4 and 6-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 7* is/are allowed.

6)☒ Claim(s) *1-4 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office action is responsive to amendment filed on 05/18/2004.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,940,055) in view of Tanaka et al. (U.S. Patent No. 5,867,139).

Regarding claim 1, referring to Fig. 3, Lee teaches a method of driving a liquid crystal display device (i.e., LCD 600), wherein the liquid crystal display device includes a gate line (i.e., gate lines G1, G2); a data line (i.e., data lines D1, D2) crossing the gate line; a dummy gate line (i.e., dummy gate line G0) adjacent the gate line; a thin film transistor (i.e., TFT11, TFT12) connected to the gate and data lines; a first capacitor (i.e., liquid crystal elements Clc11, Clc12) receiving signals from the thin film transistor; and a storage capacitor (i.e., storage capacitors Cst11, Cst12) connected between the first capacitor (i.e., liquid crystal elements Clc11, Clc12) and a previous gate line (G0), wherein a portion of the dummy gate line is an electrode of the storage capacitor (i.e., storage capacitors Cst11, Cst12), the method comprising applying a gate signal (Vgi) to the gate line (i.e., gate lines G1, G2) and applying a dummy gate signal (Vg0) to the dummy gate line (i.e., dummy gate line G0) (from col. 5, line 10 to col. 6, line 17).

Lee differs from claim 1 in that he does not specifically teach dummy gate signal is a logic high signal and the dummy gate signal has a substantially same waveform as the gate signal applied to the gate line. However, referring to Figs. 1 and 2, Tanaka teaches dummy gate signal (i.e., scanning signal G0) is a logic high signal (positive voltage level, G-0, Fig. 2) and the dummy gate signal has a substantially same waveform as the gate signal (i.e., normal scanning signals G1, G2, G3,...) applied to the gate line (3-1, 3-2,...) (col. 7, lines 21-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dummy gate signal is a logic high signal and the dummy gate signal has a substantially same waveform as the gate signal applied to the gate line as taught by Tanaka in the system of Lee in order to prevent non-uniform brightness in the display area.

Regarding claims 2 and 3, the combination of Lee and Tanaka teaches the gate signal (G1, G2...) is a pulse signal having a high period of one horizontal line period (1H) (Figs. 2 and 7 of Tanaka).

Regarding claim 4, the combination of Lee and Tanaka teaches the high period of the dummy gate signal (G0) precedes the high period of the gate signal by one horizontal line period (Fig. 2, col. 7, lines 21-47 of Tanaka).

4. Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,940,055) in view of Lee et al. (U.S. Patent No. 5,946,068).

Regarding claim 8, referring to Fig. 3, Lee teaches a method of driving a liquid crystal display (i.e., LCD 600) comprising generating a plurality of data signals corresponding to a plurality of gate signals; applying the generated data signals (i.e., signals from data driver 300) to one of a plurality of data lines (i.e., data lines D1, D2); and applying the generated gate signals

(Vg1, Vg2...) to one of a plurality of gate lines (G1, G2,...) (from col. 5, line 10 to col. 6, line 17).

Lee differs from claim 8 in that he does not specifically teach applying generated gate signals is input to a dummy gate line, and the corresponding data signal is invalidated. However, referring to Fig. 3, Lee et al. teaches applying generated gate signals is input to a gate line (i.e., gate line G1), and the corresponding data signal (i.e., dummy data line 30) is invalidated (col. 3, lines 24-58). Although, Lee et al. does not specifically teach the gate line is a dummy gate line. However, it would have been obvious to obtain the gate line is a dummy gate line in order to prevent non-uniform brightness in the display area. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the applying generated gate signals is input to a dummy gate line, and the corresponding data signal is invalidated as taught by Lee et al. in the system of Lee in order to reduce power consumption of the display device.

5. Claims 6 and 7 are allowed.

6. Applicant's arguments with respect to claims 1-4 and 6-8 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. The prior art made of record and not relied upon is considered to pertinent applicant's disclosure.

Moon (U.S. Patent No. 5,926,173) teaches circuit for driving LCD.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225.** The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, DC. 20231

**Or faxed to: 703-872-9306 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

JNguyen
08/02/2004

REGINA LIANG
PRIMARY EXAMINER